BROADBAND MONOLITHIC LOW-NOISE FEEDBACK AMPLIFIERS

P.N. Rigby, J.R. Suffolk and R.S. Pengelly

Plessey Research (Caswell) Limited,
Allen Clark Research Centre
Caswell, Towcester, Northants, England.

ABSTRACT

A 0.6 to 6 GHz monolithic GaAs FET low-noise feedback amplifier has been developed. This amplifier chip has a gain of 6 dB and a noise figure of around 4 dB over the bandwidth. Gains of 8 dB have been achieved at $\frac{1}{2}I_{dss}$ with 1 dB gain compression points of 21 dBm over the band. This paper discusses the design of such amplifiers using as an example a 1 to 10 GHz two stage monolithic amplifier chip presently under development which is capable of being cascaded up to total gains of 50 dB or so with $\pm$ 1.5 dB ripple.

INTRODUCTION

The amplification of microwave signals in a single ultra-wideband amplifier is attractive to various systems designers involved in electronic countermeasures and surveillance. In addition such amplifiers, featuring low noise figure and high 1 dB output compression points find a variety of applications as general purpose components in microwave systems.

The purpose of this paper is to describe the design of decade bandwidth monolithic amplifiers developed for the .6 to 6 GHz or 1 to 10 GHz frequency bands. The paper summarises the requirements for the MESFETs used in these amplifiers as well as giving details of the design techniques used. Monolithic chip realisations of the 0.6 to 6 GHz amplifier are described in detail together with the design and fabrication details of a 1 to 10 GHz two-stage chip.

MESFET DEVICE REQUIREMENTS

The parasitic elements of a GaAs MESFET, restrict the performance of amplifiers fabricated using the transistor. The gate-to-source and drain-to-source capacitances restrict the bandwidth of the amplifier whilst the gate-to-drain capacitance restricts the useful upper cut-off frequency of the amplifier. By applying controlled amounts of external drain-to-gate feedback to the MESFET with frequency, the gain of the MESFET can be made almost constant with frequency. In addition by correct choice of feedback resistance, feedback inductance and drain inductance the terminal VSWRs and noise figure of the amplifier can be made acceptably low for a given FET structure (1,2).

To a first approximation the forward gain of a feedback amplifier is given by

$$S_{21} = \frac{2(1 - g_m R_{FB})}{2 + (g_m + {}^1/R_o)\, Z_o + \frac{R_{FB}}{Z_o}(1 + \frac{Z_o}{R_o})}$$

For a 900 micron gate width MESFET, $g_m \approx 80$ mS at low noise bias and R_o (drain to source resistance) is 120 ohms. It is easier to match the output of the MESFET to 50 ohms than the input for a particular high g_m transistor. For $S_{22} = 0$, $S_{21} = 1-(g_m + {}^1/R_o) Z_o$ and

$$S_{11} = \frac{(g_m + {}^1/R_o)\, Z_o^2}{(1 + g_m Z_o) R_o} \quad \text{where} \quad R_{FB} = \frac{g_m + {}^1/R_o}{1 - Z_o/R_o} Z_o^2 ,$$

being the feedback resistor.

Thus, R_{FB} = 378 ohms
S_{11} = 0.37
and S_{21} = 5.3 dB.

For $S_{11} = S_{22}$, at low frequencies, R_{FB} = 221 ohms resulting in an S_{21} of 4.2 dB and $S_{11} = S_{22} = 0.145$.

GAIN BANDWIDTH OF FEEDBACK AMPLIFIERS

In order for the bandwidth of the feedback amplifier to be maximised for a given transistor an inductance or high impedance transmission line L_D in the drain line and a feedback inductance or high impedance transmission line L_{FB} are required (Fig. 1). L_D compensates for the drain-to-source capacitance of the MESFET at the upper band edge whilst L_{FB} adjusts the S-parameters of the feedback amplifier so that optimum positive feedback occurs at the upper band edge. Further amplifier performance improvements can be produced by using simple matching networks at the input and output of the FET to supplement the feedback network. For monolithic amplifiers these additional networks should be kept as simple as possible to reduce GaAs usage as well as being low-pass enabling the low frequency performance of the amplifier to be limited only by d.c. blocking and feedback capacitances.

The best performance from such amplifiers has been found to occur for MESFETs whose S_{11} and S_{22} phase angles never exceed -180^0 at the highest frequency of operation (3).

For this reason several low parasitic, high g_m FETs were designed and their S-parameters, noise figure parameters and power handling capabilities measured up to 18 GHz.

Four MESFETs shown in Table 1 have been compared for their parasitic component characteristics. The Z584 type MESFET is a physically much smaller device than the GAT6/3, the latter being the Plessey commercially available device paralleled up three times in a monolithic format. For a given carrier concentration and total gate width, the gate-to-source C_{gs}, and gate-to-drain C_{dg}, capacitances are proportional to the gate length. Comparing the Z584, 1 micron and 0.5 micron gate length versions it can be seen that C_{gs} is proportional to gate length. C_{dg} is however dominated by the geometry of the device and the contribution due to covering the FET channels with polyimide dielectric prior to the source interconnect stage. A truly airbridged source FET, the SOFET, has a C_{dg} per mm of approximately 60% that of the Z584 design indicating the dependence on MESFET layout and construction.

The importance of the value of C_{dg} can be clearly seen by inspection of Fig. 2. This figure shows the maximum available gain of the Z584/0.5 FET having a gate length of 0.5 micron as a function of feedback capacitance. The MAG at a feedback capacitance of 0.095 pF is only 3.5 dB at 18 GHz. Increasing the physical spacing between the gate and drain electrodes and removing the polyimide from the channel area results in a decreased feedback capacitance of 0.055 pF giving an MAG of 6 dB at 18 GHz. Fig. 3 shows the measured MAG of the Z584/0.5 device up to 18 GHz as well as that for the Z584/1, the 1 micron gate length version of the same basic design. The effect of C_{gs}, C_{ds} and C_{dg} can be seen clearly. Fig. 4 shows the equivalent circuits of these two MESFETs.

NOISE FIGURE OF FEEDBACK AMPLIFIERS

A feedback amplifier having no other passive matching depends for its noise figure on the MESFET and the value of the feedback resistor in the feedback path. In the limit where the feedback resistor is not present the noise figure of the amplifier becomes that of the MESFET working into a characteristic impedance, Z_o (50 ohms). A considerable number of papers have

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been written on calculating the noise figure of feedback amplifiers having both series and shunt feedback paths. This paper attempts to provide a simple means of estimating the noise figure of amplifiers using various geometry FETs. The feedback amplifier can be considered as two noise blocks. The noise figure of block 1 (the feedback resistor) is given by (4)

$$F_1 = 1 + \frac{\left|\frac{1}{R_o} + g_m\right|^2 R_o}{\left(g_m - \frac{1}{R_{FB}}\right)^2 R_{FB}}$$

where R_o is the drain to source resistance

g_m is the transconductance, and

R_{FB} is the feedback resistor.

Considering block 2 alone (the device) having a noise figure F_2 where F_{50} is defined as the 50 ohm noise figure of the MESFET, it can be shown that:

$$\frac{F_{2-1}}{F_{50-1}} \simeq 1.5$$

The 50 ohm noise figure is directly related to the noise resistance of the MESFET. From Fukui's theory (5)

$$R_n \propto \frac{1}{g_m^2} \propto \frac{1}{W_g^2} \left(\frac{aL_g}{N}\right)^{2/3}$$

where W_g is the total gate width, L_g is the gate length, a is the effective channel thickness and N is the carrier concentration in the channel.

The minimum noise figure is given by

$$F_{min}-1 \propto f C_{gs}\sqrt{\frac{R_g + R_s}{g_m}}$$

$$\propto f L_g \sqrt{g_m(R_g + R_s)}$$

The total noise figure of the transistor with resistive shunt feedback is given by

$$F_T = 1 + \sum_{i=1}^{2} (Fi-1)$$

Table 2 compares the estimated feedback amplifier noise figures at 3 GHz for three MESFETs of gate lengths 0.5, 0.7 and 1 micron. In order to allow maximum bandwidth with acceptable gain ripple and input and output VSWRs the 1 micron gate length MESFET can only have a total gate width of 450 micron resulting in a low-noise biased g_m of 40 mS. The effect of such a gate width device on feedback amplifier noise figure is demonstrated clearly. Table 2 also indicates the penalty in noise figure brought about by choosing the feedback resistor value to give the lowest simultaneous S_{11} and S_{22}. This simple method of calculating amplifier noise figure has been used to check two previously published results (2,6) at 3 GHz. These are also given in Table 2. Agreement is acceptable. The noise figure can also be estimated as a function of frequency where it is assumed that the noise resistance R_n is frequency independent. The noise figure so calculated will be a maximum figure particularly at the highest frequency since the reactive matching, particularly the drain transmission line, present in an actual amplifier will lower the noise figure (2).

Fig. 5 shows a theoretical plot of noise figure versus frequency for a 1200 micron gate width device for 0.5 and 1.25 micron gate length versions. Measured noise figures are also included showing the good agreement with theory. For the monolithic 0.6 to 6 GHz feedback amplifier described later in this paper a noise figure of 3.5 dB is estimated at 1 GHz whilst at 6 GHz this has risen to 4.2 dB. Fig. 6 shows a comparison of the gains and noise figures of two feedback amplifiers employing MESFETs of different total gate widths and lengths.

AMPLIFIER DESIGNS

In order to obtain acceptably low noise figures, 900 micron gate width FETs employing gate lengths of 0.7 and 0.5 micron have been used in monolithic feedback amplifiers enabling bandwidths of greater than 6 and 10 GHz to be realised respectively.

0.6 to 6 GHz Monolithic Amplifier

The device selected for this amplifier was the GAT6/3, which is three Plessey GAT6s connected in parallel, modified for use in monolithic circuits by removing the extra source pad area, used in the discrete device for bonding. In the monolithic version the sources are all interconnected by an air bridge. The circuit diagram for this amplifier is shown in Fig. 7. Lengths of high impedance transmission line have been used to realise 'inductors'. The feedback loop comprises such a length of line in series with a cermet resistor and an overlay silicon nitride capacitor. The smaller value shunt capacitors in the input and output matching circuits have been realised using an interdigital structure. The gate bias is fed in through a high value cermet resistor. A similar method was considered for the drain bias, but a resistor capable of dissipating sufficient heat (up to 350 mW) would have occupied a significant proportion of the total chip area. After considering alternative methods for supplying the drain bias it was found that any satisfactory method would require an unreasonably large area of GaAs, and so it was decided to have part of the bias circuit off-chip. A 5 nH spiral inductor is included on the chip and a further 10 nH are off-chip. The overall chip size is 2.8 mm x 1.8 mm and a photograph of the chip is shown in Fig. 8.

The circuits were fabricated on 200 micron thick GaAs with epitaxially grown buffer and active layers the latter being doped to 1.5×10^{17} cm^{-3}. The active device uses 0.7 micron long recessed gates and comprises six identical cells each one having two 75 micron wide gate stripes making a total gate width of 900 micron. The source and drain contacts are defined using a float off process, as is the lower metallisation, used for the interdigital capacitors in the input and output matching circuits and the bottom plates of the overlay capacitors. A thin layer of silicon nitride, used as the dielectric for the overlay capacitors, is deposited using plasma enhanced CVD and defined by plasma etching.

A layer of polyimide is spun over the wafer through which via holes are plasma ashed to form contacts between the cermet resistors and the lower metallisation. The cermet is deposited by r.f. sputtering and defined by ion beam milling using the polyimide layer as a barrier. A second polyimide layer is spun on top of the first thus sandwiching the cermet and forming a protective layer. Coincident via holes are ashed through the separate polyimide layers to enable interconnections to be made between the lower and upper metallisations, the latter being deposited by r.f. sputtering to a thickness of 3 micron and defined by ion beam milling. This upper metallisation is used as the top plate for the silicon nitride capacitors and also the lengths of transmission line and the spiral inductor in the drain bias circuit. An air bridge technology is used to connect to the centre of this spiral and also to connect together the individual sources of the FET. Finally, the polyimide is removed over the interdigital capacitors to improve their Q-factors.

The measured performance of this circuit is shown in Fig. 9 for two different bias levels. At I_{dss} the gain is 7.9 ± 0.6 dB from 1 GHz to 5.7 GHz. The output VSWR is better than 2:1 over this frequency range and the input VSWR rises to 3.2:1 at the top end of the bandwidth. It is a characteristic of these broadband feedback amplifiers that the input is more difficult to match resulting in higher input than output VSWRs. At low noise bias the measured gain is 5.8 ± 0.6 dB from 0.6 GHz to 6.1 GHz and the noise figure rises from 4.0 to 4.4 dB over this frequency range. (These results are obtained from circuits whose devices had lower than expected values of g_m and it is reasonable to assume that an improvement in gain flatness and high frequency response will be obtained from further batches currently being processed). The power gain transfer curve for this amplifier at 5 GHz is shown in Fig. 10(a) indicating a 1 dB power compression point of 21 dBm. The use of feedback also improves the intermodulation distortion and Fig. 10(b) shows the level of the third order intermodulation distortion products at 2 GHz, where the feedback is fully effective. For input signals at 2.0 GHz and 2.1 GHz and an output power of 10 mW the level of these IMD products is 50 dB below the carriers. The corresponding third order intercept point was 27 dBm.

1 to 10 GHz Monolithic Amplifier

Fig. 11 shows the predicted gain and VSWR performance of a single stage feedback amplifier employing a 450 micron gate width, 1 micron gate length MESFET. Although amplifiers based on such devices would be preferred for yield and d.c. power consumption reasons their terminal characteristics with the simple matching networks shown in Fig. 12 do not allow cascades of chips to be used without incurring unacceptable gain ripples for total gains of more than 20 dB. The only concession to off-chip tuning

allowed in the amplifiers is a variation in the length of 50 ohm microstrip lines between the chips. The input VSWR in particular is clearly unacceptable (Fig. 11). In contrast Fig. 12 shows the predicted response of a similar cascade of chips employing the 900 micron, 0.5 micron gate length transistor discussed earlier in this paper. To aid gain flatness small amounts of series feedback are included in the FET sources as well as gate inductances. The circuit diagram of the two stage chip is also shown in Fig. 12. Each chip contains five silicon nitride MIM capacitors, two 5 pF values in the feedback paths and 5 and 10 pF values for d.c. blocking. Polyimide dielectric MIM capacitors are used for the tuning capacitors where tolerances ± 10% can be achieved from batch to batch. Such a tolerance is acceptable for the amplifier. Because of the small overall size of the transistor, shown in close-up in Fig. 13, only a single ground is used enabling a simple feedback topology with no need for through-GaAs vias. Lumped inductances are replaced with meandered high impedance (85 ohm) transmission lines. The feedback and gate resistors are cermet types, the gate resistors being 2 Kohm in value. The ohms per square of the resistors is 50 ohm/sq. The drain bias to each stage is provided by two on-chip 5 nH spiral chokes having resonant frequencies beyond 10 GHz. These employ underpassed centre arm connections with polyimide separation between metal layers. The remainder of the bias network consisting of a further 10 nH inductor and capacitor are off-chip.

A composite drawing of the various mask layers is shown in Fig. 14. The two stage chip size is 1.5 x 4 mm. This chip is undergoing processing at the time of writing. It is believed that this is the first ultrabroadband low noise two stage monolithic amplifier which has been designed specifically for cascadability up to 50 dB gain.

TABLE 1: Normalised Equivalent Circuit Parameters for 4 Different MESFETs

Parameter	MESFET Type GAT6/3	Z584/1	Z584/0.5	SOFET
W_g (μm)	900	900	900	900
L_g (μm)	0.7	1	0.5	1.2
G_m/W mS/mm	80	89	80	60
C_{gs}/W pF/mm	1	1.17	0.58	0.95
C_{gd}/W pF/mm	.05	0.13	0.1	.08
C_{ds}/W pF/mm	0.4	0.2	0.2	0.275

TABLE 2: Calculated Noise Figures at 3 GHz for Feedback Amplifiers as a Function of MESFET Type

MESFET	Feedback Resistor (ohms)	Noise Resistance, R_n	Noise Figure dB	Gate Width μm	Gate Length μm
GAT6/3	250	8	3.9	900	0.7
Z584/0.5	197*	6.4	4.5	900	0.5
Z594/0.5	300	6.4	3.9	900	0.5
Z584/1	110*	40.6	8.8	450	1.0
Z584/1	328	40.6	5.8	450	1.0

MESFET	Freq. GHz	Feedback Resistor (ohm)	G_m mS	Calculated Noise Figure (dB)	R_n ohms	Published Noise Figure (dB)	Gate Width μm	Gate Length μm
WJ-F810	3	200	57	4.5	22	4.0	800	1
Rockwell	2	375	75	3.4	7	3.6	1200	1

*Feedback resistor values for lowest simultaneous $S_{11} = S_{22}$

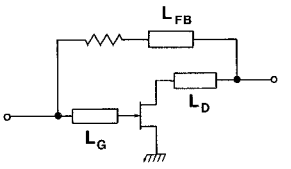

FIG. 1. Basic parallel feedback amplifier

SUMMARY

This paper has described the design, fabrication and results of monolithic feedback amplifiers covering 0.6 to 6 GHz and 1 to 10 GHz. It has been shown that with optimized MESFET geometries bandwidths up to 18 GHz are feasible. Feedback amplifiers, although not offering the lowest noise figures are capable of providing general purpose and ultrawideband units which can be readily cascaded.

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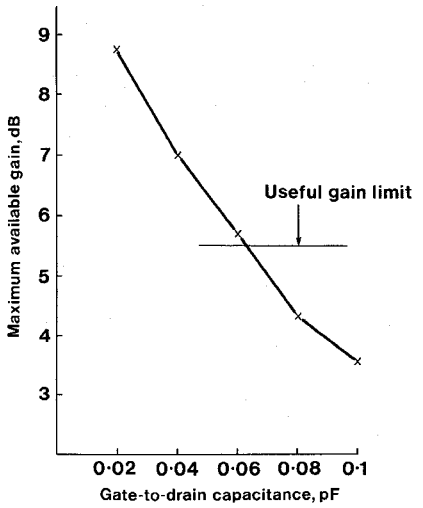

FIG. 2. Maximum available gain of MESFET as a function of gate-to-drain capacitance (W_g = 900 micron, L_g = 0.5 micron)

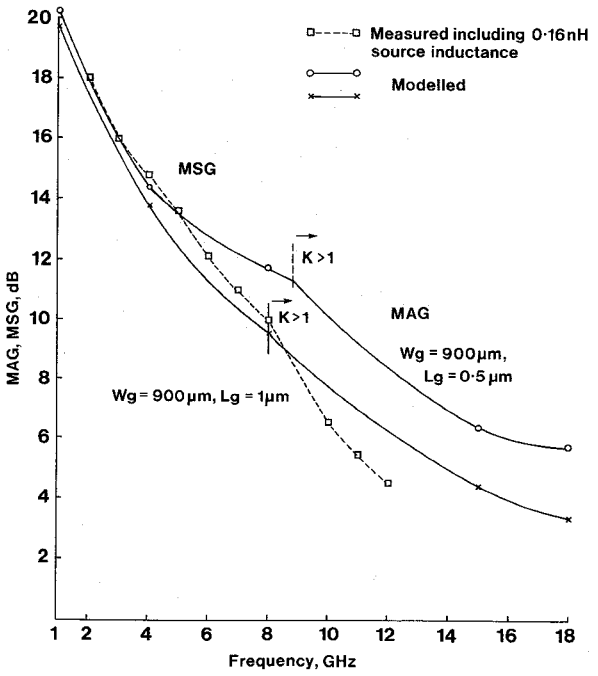

FIG. 3. Measured and modelled MAG for 900 micron gate width MESFETs as a function of gate length

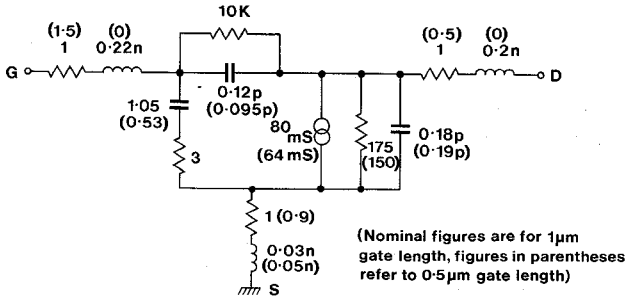

FIG. 4. Equivalent circuits of 900 micron gate width MESFETs

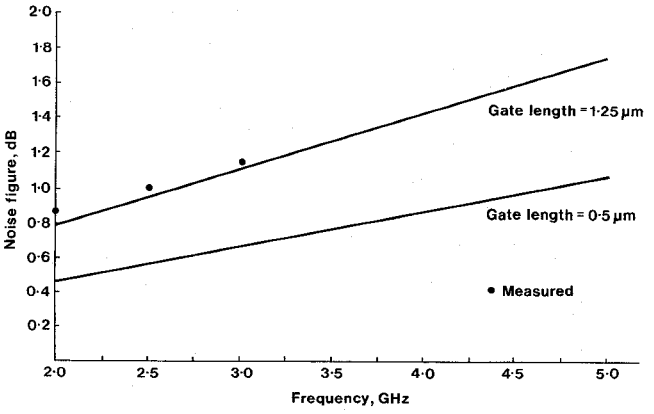

FIG. 5. Noise figure variation vs gate length for 1200 micron MESFET

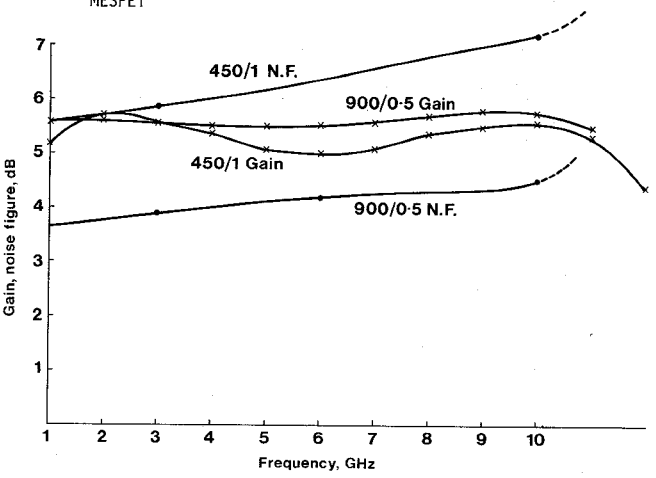

FIG. 6. Gain and maximum noise figure of feedback amplifiers

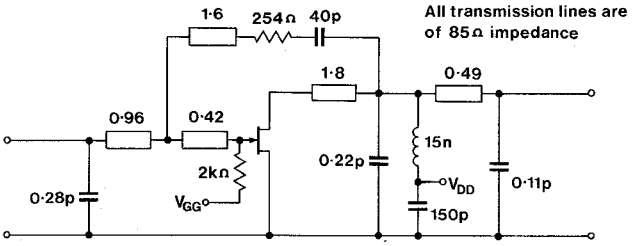

FIG. 7. Circuit diagram for monolithic 0.6 to 6 GHz amplifier

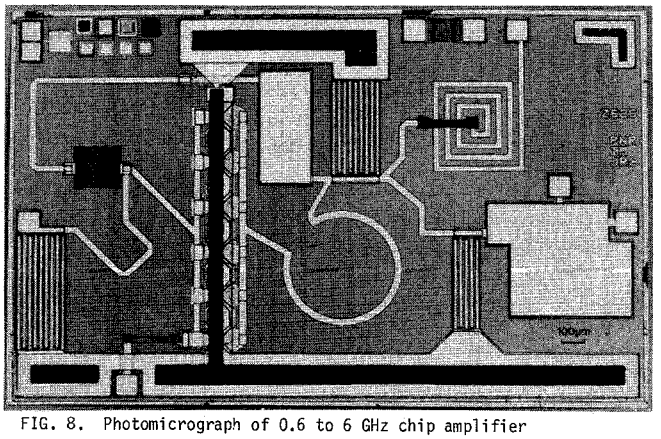

FIG. 8. Photomicrograph of 0.6 to 6 GHz chip amplifier

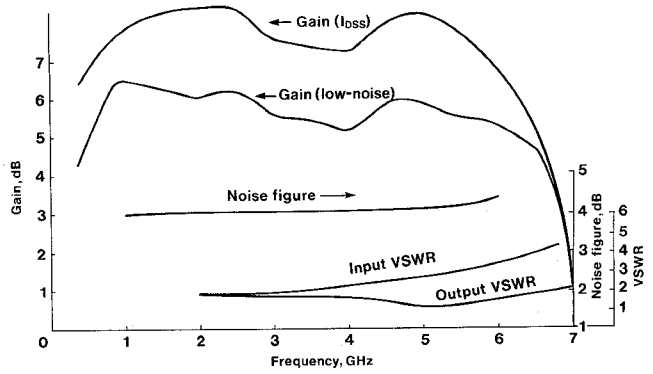

FIG. 9. Measured performance of monolithic 0.6 to 6 GHz amplifier

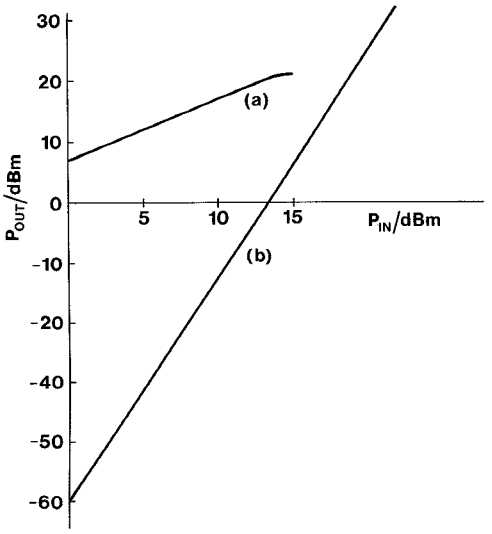

FIG. 10. (a) Power transfer characteristic and (b) 3rd order IMDs of monolithic 0.6 to 6 GHz amplifier

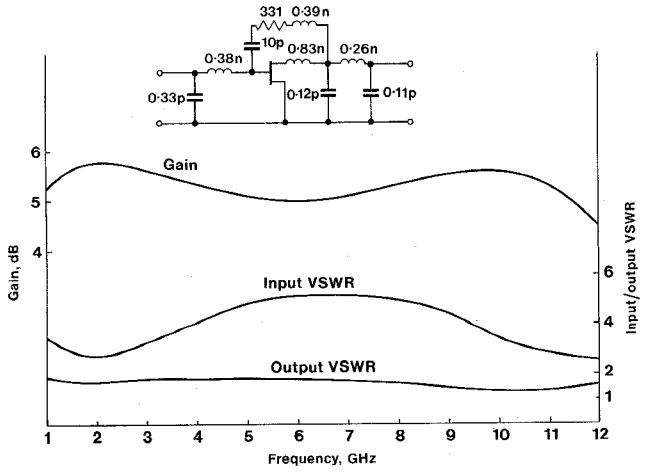

FIG. 11. Circuit diagram for 1-11 GHz feedback amplifier (W_g = 450 micron, L_g = 1 micron)

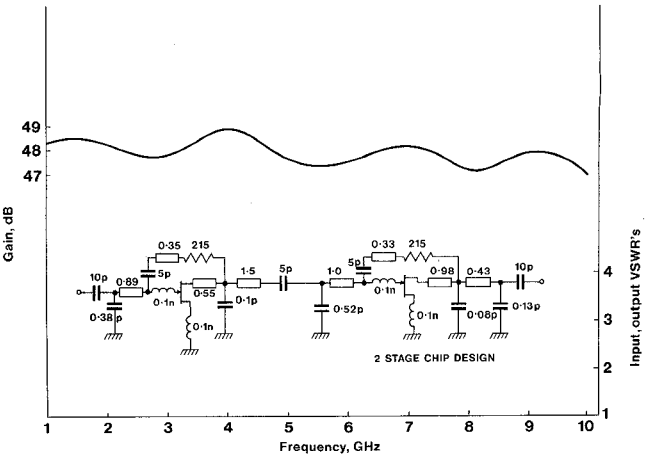

FIG. 12. Response of 4, 2 stage chips directly cascaded (2 stage chip design inset)

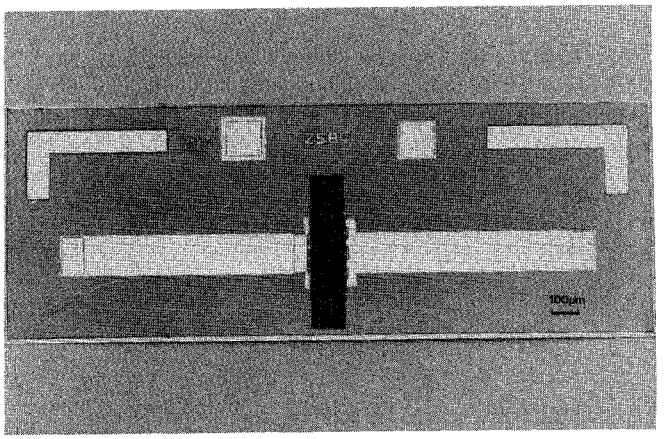

FIG. 13. High g_m, low parasitic monolithic FET

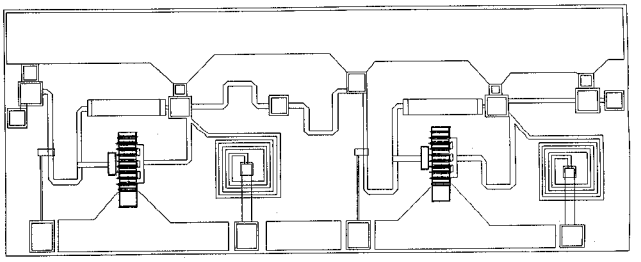

FIG. 14. Chip layout of 1 to 10 GHz low-noise monolithic amplifier.